

CLAIMS:

1. A chip 100 comprising:
an array of hexagonal cells 104;
a plurality of interconnects 130 including Y's 108 connecting the
5 cells in clusters 106 of three cells each wherein the cells in the clusters are
interconnected.
2. The chip of claim 1 wherein the Y connecting each cluster
has a node 114 and three interconnects connecting the node to respective ones
10 of the cells within a cluster;
wherein each Y connects each cell of its respective cell group to
the node.
3. The chip of claim 2 wherein the plurality of interconnects
15 are formed on a plurality of levels 110, 116, wherein nodes of Y's connecting
clusters of a lower level are interconnected by Y's of a higher level;
4. The chip of claim 3 wherein each of the Y's on a particular
level is oriented in a direction that is rotated by 90° from the Y's on a next
20 lower level and is rotated by 90° from the Y's on a next higher level.
5. The chip of claim 1 wherein the chip has a shape of a
convex polygon having at least five sides.
- 25 6. The chip of claim 5 wherein the polygon is symmetrical to
directions of the interconnect.
7. The chip of claim 1 wherein each of the clusters comprises
three cells arranged and routed in three symmetrical directions.

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8. The chip of claim 7 wherein the cells of each cluster are arranged and routed at directions of 0°, 60°, and 120° with respect to the node.

9. A chip 100 comprising:
5 a plurality of circuit elements 104 disposed on a layer;
a hierarchical, nonblocking interconnection architecture connecting the plurality of circuit elements;

wherein the interconnection includes a plurality of interconnects 130 joining clusters 106 of the circuit elements, and wherein the plurality of
10 interconnects form a mesh that is symmetrical with respect to directions of the interconnects.

10. The chip of claim 9 wherein the array has a non-rectilinear structure.

15 11. A method of selecting a nonblocking routing architecture including a plurality of interconnects interconnecting a plurality of cells, the method comprising:

determining a length L of each of the plurality of interconnects in
20 each of a plurality of the routing architectures;

determining a shortest route length D along the plurality of wires between each pair of cells in the plurality of cells for each of the plurality of interconnects in each of a plurality of the routing architectures;

25 multiplying L x D to determine a cost M for each of the plurality of interconnects in each of a plurality of the routing architectures;

selecting one of the plurality of architectures having the smallest M.

12. The method of claim 11 further comprising:
30 determining a derivative benefit for each of the plurality of routing architectures, where the derivative benefit is

$$I = -\frac{\Delta D}{\Delta L},$$

where ΔD represents the change of D and ΔL represents the change of L ;

selecting one of the plurality of architectures having a maximum
5 derivative benefit.

13. The method of claim 11 wherein

$L = \sum$ length of each wire; and wherein

$D = \sum_{1 \leq i < j \leq P} d_{i,j}$ for all values i and j where $d_{i,j}$ is a shortest route

10 length between a node i and a node j .

14. A method of adding an interconnect to a plurality of cells in a chip, the plurality of cells being connected by a hierarchical architecture, the method comprising:

15 selecting a location between a pair of adjacent cells wherein the pair of adjacent cells is connected to each other only at a root of the hierarchical architecture;

forming a bridge between the pair of adjacent cells at the selected location.

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15. The method of claim 14 wherein the bridge is arranged to be a shortest Euclidean distance connection between the pair of adjacent cells.

16. A multicell chip 100 comprising:

25 an interconnection architecture 130, the interconnection architecture comprising a plurality of interconnects interconnecting a plurality of cells 104, 140, the interconnects having a tree structure;

the plurality of cells including a pair of physically adjacent cells having a single lowest common ancestor;

the interconnection architecture further comprising a bridge 170 connecting the pair of adjacent cells and providing a direct connection between the adjacent cells.

5 17. A multicell chip 100 comprising:
an array 102 of cells 104, 140;
a plurality of interconnects 130 interconnecting the array of cells,
the plurality of interconnects being arranged in k hierarchical layers, adjacent
hierarchical layers comprising interconnects in respectively different
10 directions;

n-k layers comprising a connection path for providing a signal to
the k hierarchical layers;

at least one via extending from the n-k layers and through at least
one of the k layers;

15 the k hierarchical layers further comprising at least one tunnel for
detouring one of the interconnects on a hierarchical layer around the via, the at
least one tunnel including a detouring wire on a hierarchical layer connected to
the interconnect to complete a signal path.

20 18. The multicell array of claim 17 further comprising:
a bank of tunnels for detouring around a plurality of vias, each of
the tunnels of the bank being arranged in a similar pattern and each of the
tunnels including detouring interconnects routed in a hierarchical layer
different from the layer of the interconnects connected to the tunnel, the
25 detouring interconnects forming a complete signal path with the interconnects.

19. The chip of claim 4 wherein all cells are interconnected to
other cells.

30 20. The chip of claim 10 wherein the chip has a hexagonal
shape.

21. The chip of claim 16 wherein the interconnection architecture comprises an X-architecture having a root at n level, and wherein the bridge connects nodes at a level $n-2$.

5 22. The chip of claim 16 wherein the interconnection architecture comprises a H-architecture having a root at n level, and wherein the bridge connects nodes at a level $n-3$.

10 23. The chip of claim 16 wherein the interconnection architecture comprises a Y-architecture having a root at n level, and wherein the bridge connects nodes at a level $n-2$.